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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/610,217	07/05/2000	Shunpei Yamazaki	SEL 192	4725

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EXAMINER	
BOOTH, RICHARD A	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)
	09/610,217	YAMAZAKI ET AL.
	Examiner	Art Unit
	Richard A. Booth	2812

-- The MAILING DATE f this communication appears n the cover sh et with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 26 December 2002 .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-63 is/are pending in the application.

4a) Of the above claim(s) 1-28 and 34-52 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 29-33 and 53-63 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim R j ctions - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 29, 31, 33, 53-57, and 59-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al., U.S. Patent 5,643,826 in view of Fukuda et al., U.S. Patent 6,096,585 and further in view of Yen, U.S. Patent 5,348,897.

Ohtani shows the invention substantially as claimed including a pixel TFT disposed in a pixel unit comprising the steps of: forming an underlying film 202 over the substrate 201; forming an island-like semiconductor film 208 over said underlying film; forming n-type source and drain regions (212,213) for said pixel TFT; forming a protective insulating film 211 or 214 formed of an inorganic insulating material above the pixel TFT; forming an inter-layer insulation film 215 formed of an organic insulating material in close contact with said protective insulating film; and forming on said inter-layer insulating film a pixel electrode 216 having a light reflective surface and connected to said pixel TFT (see figs. 10A-10F and col. 11-line 64 to col. 13-line 55).

Ohtani lacks anticipation of forming both peripheral and pixel TFTs (although this is alluded to at col. 1-lines 13-19) using the steps of: forming n type impurity regions having a first concentration, for forming LDD regions of said n channel type TFT of said driving circuit and said pixel TFT in selected regions of said island-like semiconductor layers; forming n type impurity regions having a second concentration, for forming

source regions or drain regions outside said LDD regions by introducing an n-type impurity thereinto while covering at least said LDD regions of the pixel and peripheral transistors with resist masks; and forming a p type impurity region having a third concentration, for forming a source region or a drain region of said p channel TFT of said driving circuit in a selected region of said island-like semiconductor layers.

Fukuda et al. discloses forming both peripheral and pixel TFTs with island-like semiconductor films 72 by forming n-type impurity regions having a first concentration (see fig. 7B), for forming LDD regions of said n channel type TFT of said n channel type TFT of said driving circuit and said pixel TFT in selected regions of said island-like semiconductor layer, forming n type impurity having a second concentration (see Fig. 7G) for forming source or drain regions (91c,72c, for example) outside said n-type regions having the first concentration; and forming a p type impurity region (see Fig. 7C) having a third concentration, for forming a source region or a drain region of said p channel TFT of said driving circuit in a selected region of said island-like semiconductor layer (see Figs. 7A-7H and col. 7-lines 5-51). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the reference of Ohtani with the peripheral and pixel formation disclosed by Fukuda et al. because this provides a beneficial structure for both the pixel and driving portions while reducing the number of processing steps. Furthermore, Yen discloses masking LDD regions of a thin film transistor with a resist mask 158 while implanting to form heavily doped regions 150B (see figure 1C and col. 4-lines 59-68). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the process of Fukuda modified by Ohtani so as to include a resist mask while implanting heavily doped region because this will allow for an effective LDD transistor which is used to reduce the effects of hot carriers.

With respect to claim 31, note that the gate electrode material 211 in Ohtani et al. is aluminum which is both heat resistant and of low conductivity as defined by these broad terms. Regarding claim 33, note that Ohtani et al. suggests the use of the invention in active matrix liquid crystal displays which are commonly used in portable computers. Furthermore, with respect to various parameters such as the length of the LDD regions and the thickness of the semiconductor islands, it would have been obvious to one of ordinary skill in the art to optimize during routine experimentation the optimum value of these parameters based upon a variety of factors including current drive requirements, etc. and would not lend patentability to the instant application absent the showing of unexpected results.

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al., U.S. Patent 5,643,826 in view of Fukuda et al., U.S. Patent 6,096,585 and further in view of Yen, U.S. Patent 5,348,897 as applied to claims 29, 31, 33, 53-57, and 59-63 above, and further in view of Zhang et al., U.S. Patent 5,403,772.

Ohtani et al., Fukuda et al., and Hsu are applied as above but fail to expressly disclose where the p-type region formation is conducted after the protective film is formed so that a p type region is formed in an offset form.

Zhang et al. discloses forming a p-type transistor with an offset due to the presence of the protective film on the gates which is an anodic oxide film (see figs. 10A-10C and col. 19-line 1 – col. 20-line 8). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the primary reference of Ohtani et al. so as to implant after formation of the anodic oxide protection film because this will reduce any implant damage to the gate electrode.

Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al., U.S. Patent 5,643,826 in view of Fukuda et al., U.S. Patent 6,096,585 and further in view of Yen, U.S. Patent 5,348,897 as applied to claims 29, 31, 33, 53-57, and 59-63 above, and further in view of Yamamoto et al., U.S. Patent 5,672,523.

Ohtani et al., Fukuda et al., and Yen are applied as above but fail to expressly disclose the gate electrode formed of a heat resistant material specifically tantalum. Yamamoto et al. discloses making the gate electrode and gate bus lines of different materials, for example, the gate of tantalum and the bus lines of aluminum (see abstract). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the reference of Ohtani et al. so as to form the gate of tantalum as taught by Yamamoto et al. because tantalum forms a better anodic oxide and is a better gate material than previously used materials (see col. 2-lines 1-62).

Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al., U.S. Patent 5,643,826 in view of Fukuda et al., U.S. Patent 6,096,585 and further in view of Yen, U.S. Patent 5,348,897 as applied to claims 29, 31, 33, 53-57, and 59-63 above, and further in view of Saito et al., U.S. Patent 4,654,536.

Ohtani et al., Fukuda et al., and Yen are applied as above but fail to expressly disclose a pixel electrode containing both titanium and aluminum. Saito et al. discloses forming a pixel electrode of one or more of a variety of materials including titanium and aluminum (see col. 3-lines 63-66). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Ohtani et al. modified by Fukuda et al. and Yen so as to comprise a pixel electrode composed of titanium and aluminum as suggested by Saito et al. because Saito et al. has shown this to be a suitable pixel electrode structure.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is 308-3446. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are 308-7724 for regular communications and 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 308-1782.

Richard A. Booth
Primary Examiner
Art Unit 2812